CLAIMS

What is claimed is:

1. A method comprising:

resetting an integrated circuit (IC) device that has an analog front end (AFE) with an I/O buffer, the I/O buffer having a driver circuit to transmit a stream of information over a serial point to point link, and a receiver circuit to receive a stream of information over the link, the driver and the receiver circuits having digitally-controllable transmission line terminations, respectively, the I/O buffer having a digitally-controllable reference signal level;

automatically calibrating a plurality of impedance matching compensation values against a reference resistor, by a) calibrating a first compensation value, then b) calibrating a second compensation value, and c) calibrating a third compensation value; and

automatically applying the calibrated first, second and third compensation values to set said reference signal level, driver termination, and receiver termination, respectively.

2. The method of claim 1 wherein the applying includes combining an offset value with some of the calibrated plurality of compensation values.

3. The method of claim 1 further comprising writing to a plurality of software-accessible registers of the IC device an override compensation value, wherein the IC device, instead of applying the calibrated plurality of compensation values, applies the override compensation value to set one of the reference level, driver termination, and receiver termination in the I/O buffer.

4. The method of claim 1 further comprising automatically applying the same calibrated plurality of compensation values to set the reference level, driver termination, and receiver termination in an I/O buffer of every lane in a plurality of lanes of the link.

5. The method of claim 1 wherein the plurality of compensation values calibrated against a single reference resistor.

6. An integrated circuit (IC) device comprising:

an analog front end (AFE) having an I/O buffer, the I/O buffer having a driver circuit to transmit a stream of information over a serial point to point link, and a receiver circuit to receive a stream of information over the serial point to point link, the driver and the receiver circuits having digitally-controllable transmission line terminations, respectively, the I/O buffer having a digitally-controllable reference level;

a calibration circuit to calibrate a plurality of signal levels against an external, reference resistor using a plurality of comparators and a plurality of digitally-controllable variable-resistances; and

a state machine controller to transition through a first state, a second state, and a third state, wherein in each state, the controller is to a) signal the calibration circuit to generate one of the plurality of signal levels, b) initialize a counter, c) control one of the variable-resistances of the calibration circuit to change the generated one of the signal levels until an output of the comparator has signaled the counter to stop counting, and d) update one of i) the reference level of the I/O buffer, ii) the driver termination in the I/O buffer, and iii) the receiver termination in the I/O buffer, based on a value that is approximately the same as a stopped value of the counter,

and wherein the state machine controller enters the first state before entering the second state so that in the second state, the stopped value of the counter is obtained using the variable-resistance, in the calibration circuit, as set in the first state.

7. The IC device of claim 6 further comprising:

a plurality of software-programmable registers whose content is to signal the state machine controller to override the update in d) and instead update one of i) the reference level of the I/O buffer, ii) the driver termination in the I/O buffer, and iii) the receiver termination in the I/O buffer, based on the content of one of the registers.

8. The IC device of claim 6 further comprising:

a plurality of software-programmable registers whose content is to provide the state machine controller with an offset, and

wherein the state machine controller is to perform the update based on said value as combined with the offset.

9. The IC device of claim 6 wherein the state machine controller is to, after a power on reset of the IC device, enter an idle state in which the controller signals the calibration circuit to disable the generation of the plurality of signal levels, the controller is to then transition to an intermediate state and stay in the intermediate state for a predetermined number of clock cycles prior to entering the first state.

10. The IC device of claim 6 wherein the link has a plurality of lanes, each lane having a separate I/O buffer, and wherein the state machine controller is to update one of i) a reference level, ii) driver termination, and iii) receiver termination in the separate I/O buffer, in every lane, based on the same stopped value of the counter.

11. The IC device of claim 6 wherein the state machine controller is to enter an intermediate state while transitioning from the first state to the second state, wherein in the intermediate state the controller continues to signal the calibration circuit to generate said one of the plurality of signal levels that was generated while in the first state, and signals a second one of the plurality of signal levels to be generated.

12. A system comprising:

a processor;

main memory; and

an integrated circuit (IC) device which is communicatively coupled to the processor and the main memory and provides the processor with I/O access, the IC device having

an analog front end (AFE) with an I/O buffer, the I/O buffer having a driver and a receiver for a serial point to point link, the driver and the receiver having digitally-controllable transmission line terminations, respectively, the I/O buffer having a digitally-controllable reference level,

a standalone calibration circuit to calibrate a plurality of signals against an external, reference resistor, and

a state machine controller to transition through a first state, a second state, and a third state, wherein in each state, the controller is to control a signal generated by the calibration circuit until the signal has reached a calibrated level and then update one of i) the reference level of the I/O buffer, ii) the driver termination in the I/O buffer, and iii) the receiver termination in the I/O buffer, based on the calibrated level, and wherein the state machine controller enters the first state before entering the second state so that the calibrated level of the second state is obtained based on the calibrated level of the first state.

13. The system of claim 12 wherein the AFE has a plurality of I/O buffers, each having a driver and receiver, to support a plurality of lanes of the link, respectively, and

wherein the state machine controller is to update one of i) a reference level, ii) driver termination, and iii) receiver termination for every one of the plurality of lanes based on the same calibrated level.

14. The system of claim 12 wherein the state machine controller implements counter logic having a thermometer-encoded output that represents the signal generated by the calibration circuit.

15. The system of claim 12 wherein the IC device is part of a root complex.

16. The system of claim 15 wherein the IC device is a memory controller hub.

17. The system of claim 15 wherein the IC device is an I/O controller hub.